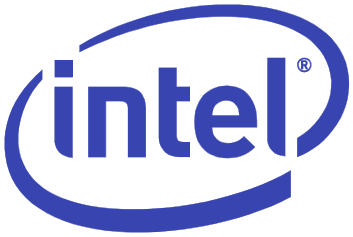

# Data Retention in Intel® Solid-State Drives

***Application Note***

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## Contents



# 1.0 Overview

Data retention is an important reliability attribute for Intel® Solid-State Drives (Intel® SSDs). This application note provides an overview of the key factors affecting data retention in solid-state drives (SSDs) and describes the JEDEC standard for SSDs: *Solid State Drive (SSD) Requirements and Endurance Test Method* (JESD218A). This application note also discusses the data retention capability of Intel SSDs for both client and data center (enterprise) applications.

# 2.0 Data Retention in Solid-State Drives

Data retention is the ability of an SSD to retain data over time.

Intel SSDs are built with NAND flash memory, a non-volatile memory component that has finite data retention capability. Once data is written in the NAND, the data will be retained only for a specific finite amount of time if the data is not refreshed or re-written.

For example, if the NAND data retention capability is specified as one year, data will be retained indefinitely provided that the NAND gets rewritten *at least* once per year. Data will be rewritten not only when the user rewrites the data, but also when internal drive algorithms move the data from one location in the SSD to another. In Intel SSDs, these internal data moves are generally sufficient to refresh the data often enough for data retention to be a non-issue in active use, even for files that are left unchanged by the user for years. Of course, such data moves are impossible when the drive is powered off. Therefore, one should view the data retention capabilities in this application note as the ability of a drive to retain data for a long time during a period of non-use. Retention during active use will be far longer, usually effectively unlimited.

Several factors impact the underlying NAND data retention capability. Key factors include:

- **Number of Program/Erase (P/E) cycles**: the number of P/E cycles performed on the NAND flash device, which is directly proportional to the total amount of data written to the SSD.
- **Storage conditions**: the storage time and temperature.
- **P/E cycling conditions**: the time duration over which the P/E cycles are performed on the NAND (which depends on the rate at which data is written to the SSD) and the temperature during P/E cycling.

The statements made in this document are strictly from a data retention point of view. Other NAND reliability mechanisms may be affected by these factors and should also be taken into consideration.

## 2.1 Data Retention Mechanisms in NAND Flash Memory

During a *program* operation of a NAND flash cell, electrons are injected through the tunnel oxide into the floating gate. During an *erase* operation, electrons are discharged through the tunnel oxide into the channel. During both of these operations, a very high electric field of more than 10 million volts per cm is generated, which can cause damage to the tunnel oxide, thus degrading the tunnel oxide quality over time.

The damage, in the form of broken bonds or *traps* in the bulk tunnel oxide or at the interfaces, leads to some electrons getting trapped at these metastable defects rather than being properly stored in the floating gate during program or data writes. These trapped electrons are unstable; they may detrap over time, resulting in data loss. This mechanism is commonly referred to as *intrinsic charge loss* (ICL), also known as *detrapping-induced charge loss*. Moreover, this charge loss mechanism is strongly thermally activated; that is, the rate of charge loss is highly dependent on temperature. Finally, some of the damage that is generated during program/erase operations recovers or heals during naturally occurring delay or dwell times between any two successive P/E cycles. This recovery mechanism is the same as the ICL mechanism itself, and thus also highly thermally activated. For an in-depth technical review of ICL, see reference papers 1 and 2 in Table 3 on page 21.

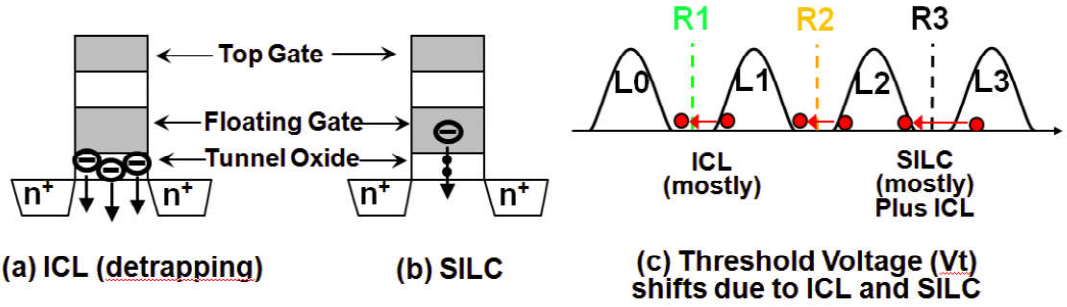
The damage introduced in the tunnel oxide from P/E cycling of NAND flash cells can also form a leakage path for the electrons stored in the floating gate, which causes another data retention issue commonly referred to as *stress-induced leakage current* (SILC). Unlike ICL, the SILC mechanism is not highly dependent on temperature, and can anneal out at relatively low temperatures (as low as 55 ºC). For an in-depth technical review of this mechanism, see reference paper 3 in Table 3 on page 21.

Figure 1(a) and Figure 1(b) show the schematic cross section of a multi-level cell (MLC) NAND flash cell, which is basically a transistor with a floating gate added to store the charge corresponding to the state of the memory cell.

- Figure 1(a) illustrates the ICL mechanism, where electrons (depicted by circles with dashes within them) trapped in the tunnel oxide are shown to detrap (indicated by the arrows), causing a net charge loss for the memory cell.
- Figure 1(b), alternatively, illustrates the SILC mechanism. It shows the leakage path created by the defects in the tunnel oxide (depicted by the two dots) which can lead to an electron in the floating gate leaking away as indicated by the arrow.
- Figure 1(c) shows the schematic for the threshold voltage (Vt) distributions in a two-bit-per-cell MLC NAND array, and the read reference voltages R1 through R3 used to distinctly sense the four levels, L0 through L3.

The ICL and SILC types of charge loss as depicted in Figure 1(a) and 1(b), respectively, are shown in Figure 1(c) to result in a Vt loss with the red arrows (the Vts corresponding to the electron before and after charge loss are shown by the red dots). When the Vt drops below the read levels (depicted by the arrow crossing the read reference voltage line), a bit failure occurs. ICL mostly results in L1-to-L0 or L2-to-L1 failures, whereas SILC (which is highly voltage accelerated) mostly results in L3-to-L2 failures.

**Figure 1. ICL, SILC, and Threshold Voltage (Vt) Shifts in an MLC NAND Flash Cell**




### 2.1.1 Impact of P/E Cycles

Both ICL and SILC data retention mechanisms originate from degradation of tunnel oxide quality over time from P/E cycling. Therefore, with all other factors such as temperature being equal, the data retention capability of NAND flash cells is greater on devices with fewer P/E cycles than on devices with a greater number of P/E cycles. So, the retention capability is in reality better over most of the use life than that specified for the maximum endurance rating. The quantitative dependence on the number of P/E cycles is typically a power law, which results in a straight line when plotted on a log-log plot, as shown in Section 4.0, “Intel SSD Data Retention” on page 12.

### 2.1.2 Impact of Storage Conditions

Data retention due to ICL in NAND is highly thermally activated as mentioned previously. At higher storage temperatures, data retention degrades, as the ICL mechanism accelerates with temperature. You can thus take advantage of this in qualification testing by emulating a long storage time at a low-use temperature with a high temperature bake. The Arrhenius Equation is used to predict the acceleration effect of storage temperature. The time acceleration factor (AF) is as follows:

#### Arrhenius Equation

$$AF = e^{\frac{Ea}{K}\left(\frac{1}{T1}-\frac{1}{T2}\right)}$$

,

- AF = Acceleration factor (a constant that relates the retention times-to-failure at two different storage temperatures T1 and T2); AF allows extrapolation of failure rates from accelerated stress test conditions to use conditions
- K = Boltzmann constant = 8.617 x 10-5 [eV/K]
- T1 = Retention or storage temperature [K] under actual use condition
- T2 = Data retention stress bake temperature [K]
- Ea = Activation energy; typically 1.1eV

#### *Example of Arrhenius Equation*

The JEDEC *Solid State Drive (SSD) Requirements and Endurance Test Method* (JESD281A) standard defines the storage use temperature for enterprise-class SSDs as 40 ºC and the retention use time requirement as 3 months (2,190 hrs).

During the data retention qualification of enterprise-class SSDs, a high-temperature data retention stress bake test is performed after the endurance stress test (with a specified maximum number of terabytes written [TBW]) to demonstrate the data retention requirement. One of the prescribed retention stress bake temperatures is 66 ºC, as specified in JESD218A, Table 3: “Endurance and retention times and temperatures by drive class”.

The bake time is calculated as follows in this example:

- T1 = 40 + 273.15 [K]
- T2 = 66 + 273.15 [K]
- Ea = 1.1 [eV]

Using the Arrhenius Equation mentioned above, AF = 22.76. The high temperature retention stress bake time = 2190 / 22.76 = 96 [hrs], which is the bake time specified in JESD218A, Table 3: “Endurance and retention times and temperatures by drive class”.

As mentioned earlier, SILC is not thermally activated (SILC has a fairly low activation energy of ~0.2eV). More importantly, the SILC mechanism can sometimes anneal out at relatively low temperatures (as low as 55 ºC), so generally a high temperature bake cannot be used to



accelerate it to emulate a use condition. JESD218A takes this into account, as explained in Section 3.0, “JEDEC Standard for SSD Data Retention,” on page 10.

### 2.1.3 Impact of P/E Cycling Conditions

The third key factor that affects data retention is how fast or slow P/E cycles are performed on the NAND flash cell. This is due to the recovery effect mentioned in Section 2.1, Data Retention Mechanisms in NAND Flash Memory,” on page 5.

With slower P/E cycles, there is more time between successive P/E cycles for the traps – introduced in the tunnel oxide during the actual program and erase operations – to recover or anneal. The delay between P/E cycles reduces the trapped charge in place at the beginning of a subsequent bake. As a result, detrapping in bake or ICL is smaller when P/E cycling is distributed over a relatively longer period of time — which is what can be expected to happen in realistic field usage — as compared to very fast P/E cycling one might be able to do in a retention qualification test, since the actual times for programming and erasing the NAND are quite small.

It is important to note that what matters is the total time to perform a given number of P/E cycles and not the individual delay times, or their maximum, between any two successive P/E cycles since the recovery effect is a cumulative effect. Since the recovery mechanism is also highly thermally activated as mentioned earlier, the P/E cycling temperature also matters in addition to the P/E cycling time. However, at *higher* P/E cycling temperatures, data retention *improves* since the recovery effect accelerates at higher temperatures, which is opposite to the effect of storage temperature. The P/E temperature acceleration factor follows the Arrhenius relationship similar to that for storage temperature, with the same 1.1eV activation energy.

The dependence of retention on the P/E cycling conditions (that is, P/E cycling time and temperature) is particularly important to keep in mind because traditionally this dependence was not thought to be a significant factor, and data retention was considered to be dependent *only* on the storage (bake) conditions. This is important not only in assessing different potential usage conditions that may be expected in a given application, but also, more importantly, with how to emulate them in qualification testing, as described in the next section.

#### *Example of Distributed P/E cycling*

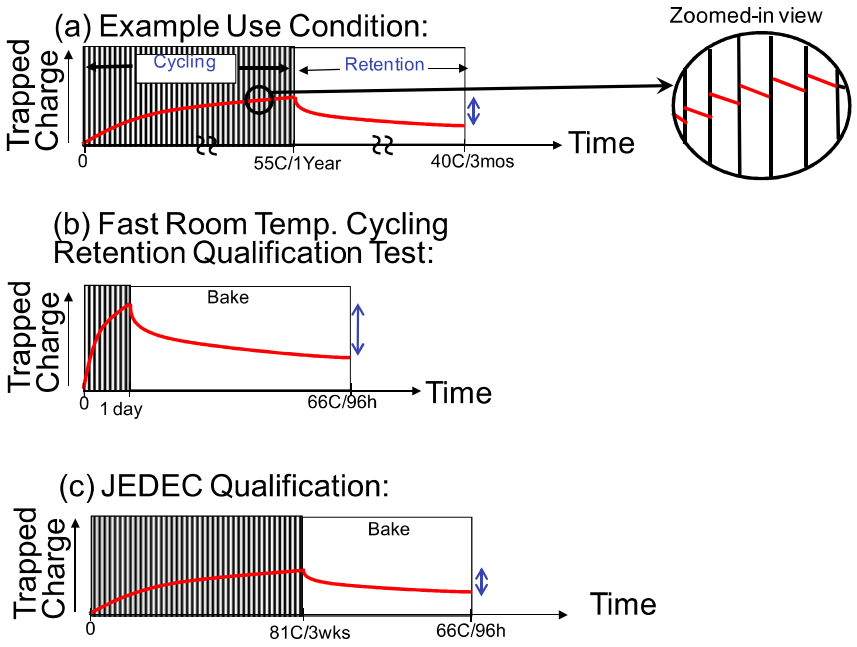
This section looks at the use scenario in the JESD218A standard for the enterprise-class SSD, as depicted in Figure 2.(a) on page 9: active use over a period of 1 year at 55 ºC during which the SSDs are written to their endurance ratings, followed by a power-off period of 3 months at 40 ºC, after which the data is still expected to be retained.

Traditionally, P/E cycling is performed as fast as possible before the retention bake (for example, in one day) to obtain the data quickly. Then, data retention can be

accelerated by choosing a high bake temperature (for example, 66 ºC), and the corresponding bake time to match the 40 ºC-3 months retention condition using a characterized activation energy $E_a$: 96hrs, as calculated in the *Example of Arrhenius Equation* on page 7.

As shown in Figure 2.(b), which depicts this scenario, the amount of detrapped charge due to ICL measured will be much larger than what might be expected in a more realistic usage condition, as depicted in Figure 2.(a); and thus, the retention capability in the use condition would be underestimated. (The two-sided, up-and-down blue arrows in the figure below depict the relative amounts of detrapped charge in the two cases.) To emulate the use condition correctly, the P/E cycling conditions should be chosen carefully, taking advantage of the strong thermal acceleration of the recovery process. To keep the total test time reasonably short, the P/E cycling time can be, for example, three weeks. To emulate the 55 ºC-1 year active use condition (during which the P/E cycling is performed), the P/E cycling temperature can be shown to be 81 ºC using the Arrhenius relationship and an activation energy $E_a$ of 1.1eV. The resulting overall test flow, which is consistent with JESD218A, is depicted in Figure 2.(c) and is the right flow to emulate the retention capability in the use condition in Figure 2.(a).

**Figure 2. Recovery Effects During Distributed P/E Cycling[1]**




1. *Recovery Effects in the Distributed Cycling of Flash Memories,* Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International.

(a) Schematic diagram of the enterprise-class SSD use condition of JESD218A. The vertical lines represent P/E cycles. The oxide trapped charge build-up during P/E cycling and its detrapping during the retention period are represented by the red curved lines. During P/E cycling (zoomed-in view), the trapped charge builds up during the program and erase operation of each P/E cycle, but partially recovers during the delay before the next P/E cycle. The amount of detrapping during the retention period is schematically depicted by the double-sided blue arrow.

(b) Traditional retention qualification, where the P/E cycling is done very fast at room temperature (RT). The charge build-up during P/E cycling and the amount of detrapping afterward is greater than it would be under the use condition.

(c) JEDEC retention qualification. The charge build-up during P/E cycling and detrapping afterward is matched to that of the use condition.



# 3.0 JEDEC Standard for SSD Data Retention

Intel follows the JEDEC *Solid State Drive (SSD) Requirements and Endurance Test Method* (JESD218A) standard which defines the endurance and data retention rating and qualification methods for the two SSD application classes: client and enterprise (data center).

JESD218A states the maximum endurance rating for an SSD should represent the maximum number of terabytes that may be written by a host to the SSD using the workload specified for the application class, known as the Terabytes Written (TBW) rating, such that the following conditions are satisfied:

a) the SSD maintains its capacity,

b) the SSD maintains the required functional failure requirement (FFR) of $\leq$3%,

c) the SSD maintains the required uncorrectable bit error rate (UBER) of $\leq 10^{-15}$ for client-class and $\leq 10^{-16}$ for enterprise-class; and

d) the SSD retains data during *power-off* for the required time for its application class.

When Intel SSD product specifications are more stringent than the JEDEC requirements, Intel qualifies SSDs to the more stringent standards. For example, the *Intel® SSD 320 Series Product Specification* states UBER of $10^{-16}$ rather than $10^{-15}$, and Intel uses the former as the requirement that must be met in SSD qualification.

The standard also specifies the endurance and retention verification approaches that may be used as part of a drive qualification. The standard is based on a use scenario in which the SSDs are actively used (powered on) for some period of time where data is written to the SSDs to the TBW rating, followed by a period of non-use (powered off) time during which data could be lost due to retention. To emulate this scenario, the endurance stress or verification step (P/E cycling) is run first followed by the retention verification step (retention bake).

For the endurance verification step, there are two methods: (1) the Direct Method, which is to be followed if the TBW rating can be reached in a reasonable time such as 1,000 hours; or (2) one from a set of Extrapolation Methods to be followed if the TBW could take a much longer time. Additionally, the endurance stress can be done using the ramped or the split approach. Intel uses the split approach. The split approach involves running two sets of drives, one at low temperature and one at high temperature, where the high temperature set continues on to the retention verification step.

Table 1 on page 11 summarizes the JEDEC standard for client and enterprise SSD application classes.

### Table 1. SSD Endurance and Retention Times and Temperatures[1]

| SSD Application Class | Workload (see JESD219) | Active Use (power-on) | Retention Use (power-off) | Endurance Stress (Cycling) Temperature ($T_{max}$ values as JESD281A) | High Temperature Retention (Storage) Stress Temperature |
|---|---|---|---|---|---|
| Client | Client | 40 °C<br>8 hours/day<br>For 1 year | 30 °C<br>1 year | Ramped approach:<br>Low: T≤25 °C<br>High: 40°C ≤T≤$T_{max}$<br>Split-flow approach:<br>Low: T≤25 °C<br>High: 40°C ≤T≤$T_{max}$ | 96 hours /<br>T≥66 °C<br>or<br>500 hours / T≥52 °C |
| Enterprise | Enterprise | 55 °C<br>24 hours/day<br>For 1 year | 40 °C<br>3 months | Ramped approach:<br>Low: T≤25 °C<br>High: 60°C ≤T≤$T_{max}$<br>Split-flow approach:<br>Low: T≤25 °C<br>High: 60°C ≤T≤$T_{max}$ | 96 hours /<br>T≥66 °C<br>or<br>500 hours / T≥52 °C |

1. Based on Table 3 and Table 4 in the JESD281A specification: *Solid State Drive (SSD) Requirements and Endurance Test Method.*

The standard provides some flexibility on the endurance stress (or P/E cycle) time in the form of a table (see Table 4 "Maximum endurance high temperature ($T_{max}$) vs. endurance stress times" in the JESD218A specification), from 50 hours to 3,000 hours. The corresponding values of $T_{max}$ have been calculated such that the endurance stress time is equivalent to one year at the active-use temperature and hours/day shown in Table 1 above, assuming an activation energy of 1.1eV, similar to the method described in "Example of Distributed P/E cycling" on page 8. And, finally, as can be seen in the last column, there are two equivalent options for the retention bake temperature, again assuming a 1.1eV activation energy.

The endurance and retention stresses in Table 1 above are designed around a high activation energy mechanism such as ICL. For low activation energy mechanisms, such as SILC, the standard suggests an optional room temperature retention verification step following the low temperature endurance verification step or to obtain that data at the NAND component level during the NAND component qualification. Both methods require mathematical extrapolations since it is difficult to accelerate the mechanism using high temperature bakes or other stresses.

See the JESD218A standard for details regarding all the different endurance and stress methods for SSD data retention briefly discussed in this section.



# 4.0 Intel SSD Data Retention

Intel adheres to the JEDEC endurance and data retention stress methods and recommendations as described in the JESD218A standard to ensure its SSDs have sufficient retention capability. The Intel® Solid-State Drive 320 Series and Intel® Solid-State Drive 710 Series both meet or exceed the JESD218A requirements, as shown in this section.

## 4.1 Endurance Ratings

The endurance rating for an Intel SSD is specified as *Endurance Rating* in terms of terabytes written or petabytes written, in the associated Intel SSD product specification. (See Section 7.0, "Additional Information" on page 21 for information on obtaining Intel product specifications.)

Intel also provides a Media Wearout Indicator (SMART attribute E9h) which reports the amount of the endurance remaining at any point in time. Intel ensures our SSDs meet or exceed JESD218A requirements at both the specified TBW rating and the point at which the Media Wearout Indicator indicates that the full endurance has been consumed.

Ideally, the Media Wearout Indicator would fall to 'empty' at precisely the moment when the total writes to the SSD reaches the TBW rating shown in the product specification, and that point would also correspond to the point at which the NAND reaches its endurance limit; however, there are two reasons why this may not be the case:

- First, the Media Wearout Indicator is based on actual P/E cycles experienced by the NAND in actual use, whereas the TBW rating is based on the P/E cycles that will occur if the SSD is used with a particular reference workload.

  An analogy is with automobiles, which have fuel gauges that report actual fuel consumed in addition to fuel efficiency ratings (miles per gallon or km per liter), which are based on an assumed workload (combination city and highway driving). One could calculate how much distance one could drive before the fuel runs out, based on the size of the tank and the rated fuel efficiency. However, in real-use situations, the fuel might run out earlier or later, depending on how the automobile is driven. This is similar with SSDs. Actual NAND P/E cycles experienced for a given TBW depend on the way in which the SSD is used. For example, long sequential writes tend to be benign (like highway driving) and short random writes tend to be harsher (like city driving). As a result, even if the TBW rating and the Media Wearout Indicator are perfectly calibrated for the reference workload, in real use one limit may be reached before the other.

  For clarity, this document refers to the TBW rating (as specified in the Intel SSD product specification as *Endurance Rating*) as simply the *TBW rating*, and the NAND limit used in the Media Wearout Indicator as the *Media Wearout Limit*. Intel ensures that our SSDs meet or exceed the JESD218A requirements at the TBW rating (assuming the reference workload) and at the Media Wearout Limit (regardless of the workload).

- Second, the TBW rating in the product specification is a conservative underestimate of the real capability of the SSD in some cases, specifically for client SSDs such as the Intel SSD 320 Series. Based on study of client usage and on collaboration with major customers, Intel believes that normal client usage involves writing 20 GB/day or less, and has chosen to rate SSDs accordingly (36.5 TB corresponds to 20 GB/day over 5 years).

  The Intel SSD 320 Series, however, is capable of even higher TBW, and the Media Wearout Indicator is based on the actual NAND capability. An Intel SSD 320 Series that reaches its TBW limit will generally show a Media Wearout Indicator that is more 'full' than 'empty'. The extent of this conservatism depends on the SSD capacity. Intel has chosen to rate all capacities of Intel SSD 320 Series at the same TBW rating, but in fact writing 36.5 TB to a large capacity SSD results in fewer NAND P/E cycles than writing 36.5 TB to a small capacity SSD.

The TBW rating for enterprise applications for both the Intel SSD 320 Series and the Intel SSD 710 Series is defined in terms of TBW that changes with the SSD capacity and is closely aligned to the Media Wearout Limit for each capacity.

## 4.2 Data Retention Test Methods

Based on SSD capability and system requirements, Intel uses different methods for testing data retention. These methods follow the recommendations of JESD218A.

For a client SSD such as the Intel® Solid-State Drive 320 Series, Intel uses the *direct* method because targets for maximum TBW specified in the product specification can be met on all NAND blocks in a reduced time. Intel also uses NAND component data to determine the Media Wearout Limit, since that exceeds the specified TBW rating.

Alternatively, with an enterprise SSD such as the Intel® Solid-State Drive 710 Series, Intel uses the reduced-capacity *extrapolation* method to achieve the high number of P/E cycles corresponding to the Media Wearout Limit on a fraction of NAND blocks.

For mechanisms not accelerated by temperature, such as SILC, Intel leverages component data.

JESD218A contains no requirement for data retention for low endurance use conditions (such as read-only workloads). However, Intel SSDs are additionally qualified for data retention of seven years for NAND blocks within SSDs that experience a low number (in the 10s) of P/E cycles.

Additionally, the Intel SSD quality and reliability verification process starts by defining the correct requirements early in the product design. The process involves comprehensive product design and technology development integration, implementation of robust and controlled manufacturing processes and systems, and ultimately leads to Quality and Reliability Verification (QRV) testing on the finished product.

For more information on Intel SSDs, go to http://www.intel.com/go/ssd.

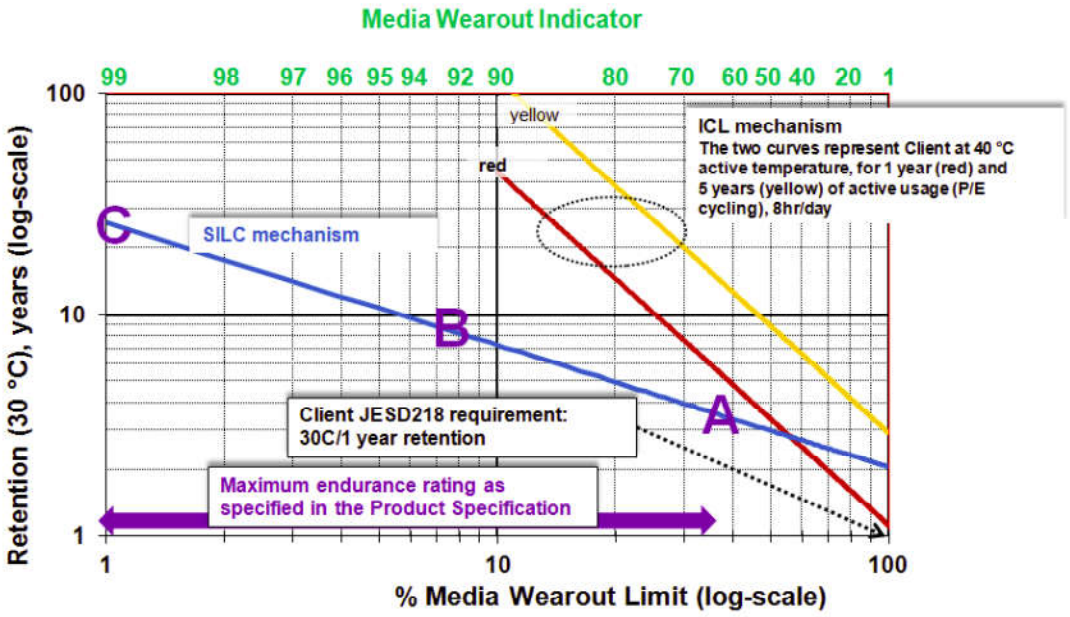
## 4.3 Data Retention – Intel® Solid-State Drive 320 Series

The data retention capability of the Intel SSD 320 Series is shown in Figure 3.

- The red line represents ICL for a P/E cycling time of 1 year at 40 ºC (JESD218A condition for client-class).
- The yellow line represents ICL for a P/E cycling time of 5 years; thus, it is shifted up from the red line due to the recovery effects mentioned earlier.
- The blue line represents SILC, which is independent of the P/E cycling time.
- The x-axis represents the number of P/E cycles seen by the NAND normalized to the Media Wearout Limit. (The x-axis could also be viewed to represent the Media Wearout Indicator, as shown in green at the top of the plot.)

Figure 3 shows that at 100% of the Media Wearout Limit, the 30 ºC retention times due to SILC and ICL (red line) are about 2 years and just above 1 year, respectively, and the overall retention capability is 1 year, limited by ICL.

**Figure 3. Data Retention – Intel SSD 320 Series**



The two-sided purple arrow shows the percentage of Media Wearout Limit for various capacities of the Intel SSD 320 Series and usage conditions for *client* applications. It can be seen that the retention ranges from about 3.5 years to greater than 25 years, which is much greater than the 1 year specified by JESD218A; the overall retention in this range is limited by SILC and not ICL.

For example:

(A) The extreme right end of the range corresponds to a 40 GB Intel SSD 320 Series and a 5 years useful life over which the data is written at the rate of 20 GB/day. The number of P/E cycles on the NAND in this case is only 36.5% of the Media Wearout Limit. At this point, the retention due to SILC (blue line) is about 3.5 years (as denoted by letter A in Figure 3) and that due to ICL (yellow line) is about 15 years; therefore, overall retention is about 3.5 years, which is much higher than the 1 year specified by JESD218A.

(B) If we consider instead a useful life of 1 year, which makes the ICL retention worse (red line), the number of P/E cycles drops to 7.5% and the retention is even better, between 8 and 9 years (as denoted by letter B in Figure 3); the ICL becoming worse in this case does not matter since the overall retention is limited by SILC.

(C) For the largest capacity 600 GB Intel SSD 320 Series (and still 20GB/day for a useful life of 1 year), the number of P/E cycles drops to less than 1% of the Media Wearout Limit, and the retention is greater than 25 years (as denoted by letter C in Figure 3).

In summary, the Intel SSD 320 Series not only meets but also exceeds the minimum JESD218A client-class requirement of 1 year retention at 30 ºC for both the TBW rating and the Media Wearout Limit.

***Note:*** The Intel SSD 320 Series can also be used in data center (enterprise) applications, where the TBW rating is closely aligned with the Media Wearout Limit. Though the corresponding data retention capability is not shown in Figure 3, the Intel SSD 320 Series not only meets but also exceeds JESD218A enterprise-class retention requirement.

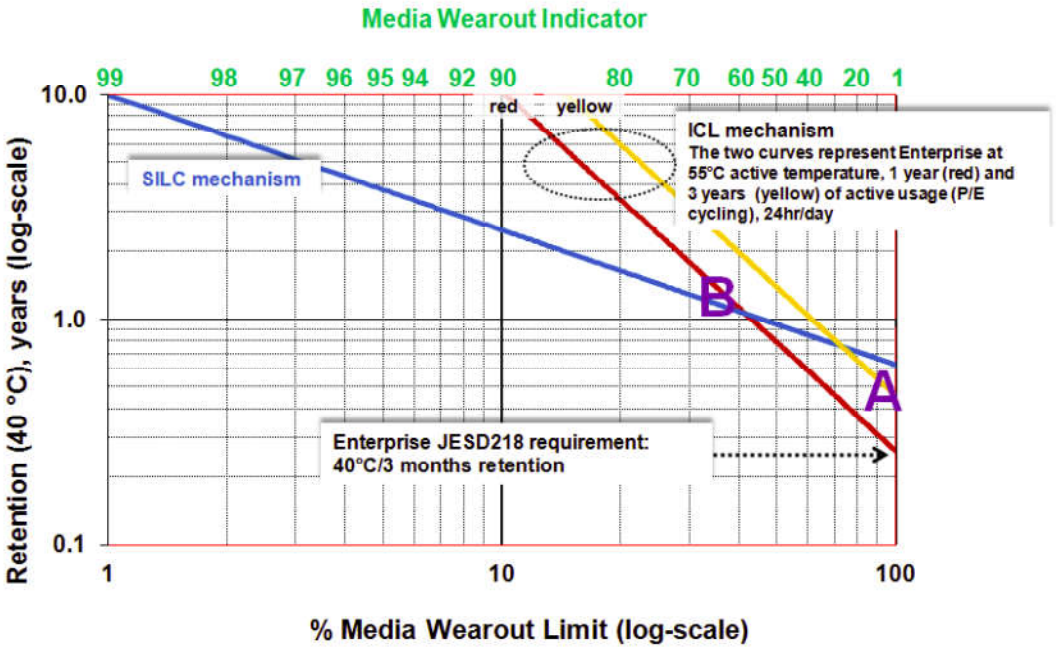
## 4.4 Data Retention – Intel® Solid-State Drive 710 Series

The data retention capability of the Intel SSD 710 Series is shown in Figure 4, which is similar to Figure 3 on page 14.

- The red line represents ICL for a P/E cycling time of 1 year at 55 ºC (JESD218A condition).
- The yellow represents ICL for a P/E cycling time of 3 years, thus it is shifted up from the red line due to the recovery effects mentioned earlier.
- The blue line represents SILC, which is independent of the P/E cycling time.
- The x-axis represents the number of P/E cycles seen by the NAND normalized to the Media Wearout Limit (which is closely aligned to the TBW rating in this case). The Media Wearout Indicator itself is also shown (in green) at the top of the plot.

Figure 4 shows that at 100% of the Media Wearout Limit, the 40 ºC retention times due to SILC and ICL are about 7 months and 3 months, respectively, and the overall retention capability is 3 months, limited by ICL.

**Figure 4. Data Retention – Intel SSD 710 Series**



In the case of the Intel SSD 710 Series, overall retention capability is limited by either ICL or SILC, depending on the usage conditions.

For example:

(A) The number of P/E cycles corresponding to the TBW of 900 TB specified in the *Intel® Solid-State Drive 710 Series Product Specification* for a 100 GB capacity SSD is close to 100% of the Media Wearout Limit. However, since it realistically corresponds to host writes done over a period of 3 years, the ICL retention capability (yellow line) is about 5.5 months, denoted by the letter A in Figure 4. The retention due to SILC is greater, about 7 months, and the overall retention is limited by ICL in this case, about 5.5 months, which is much higher than the 3 months specified by JESD218A.

(B) Alternatively, considering the same 100 GB SSD but in the case where data is written to the SSD at the same rate but over a period of 1 year instead of 3 years, the number of P/E cycles would be at about 33% of the Media Wearout Limit. As denoted by letter B in Figure 4, the retention in this case would be 1.3 to 1.5 years, and be limited by both SILC and ICL (red line).

In summary, the Intel SSD 710 Series meets the minimum enterprise JESD218 requirement of 3 months retention at 40 ºC, and is generally capable of better retention at more realistic usage conditions of longer than one year of active usage or smaller amount of TBW.

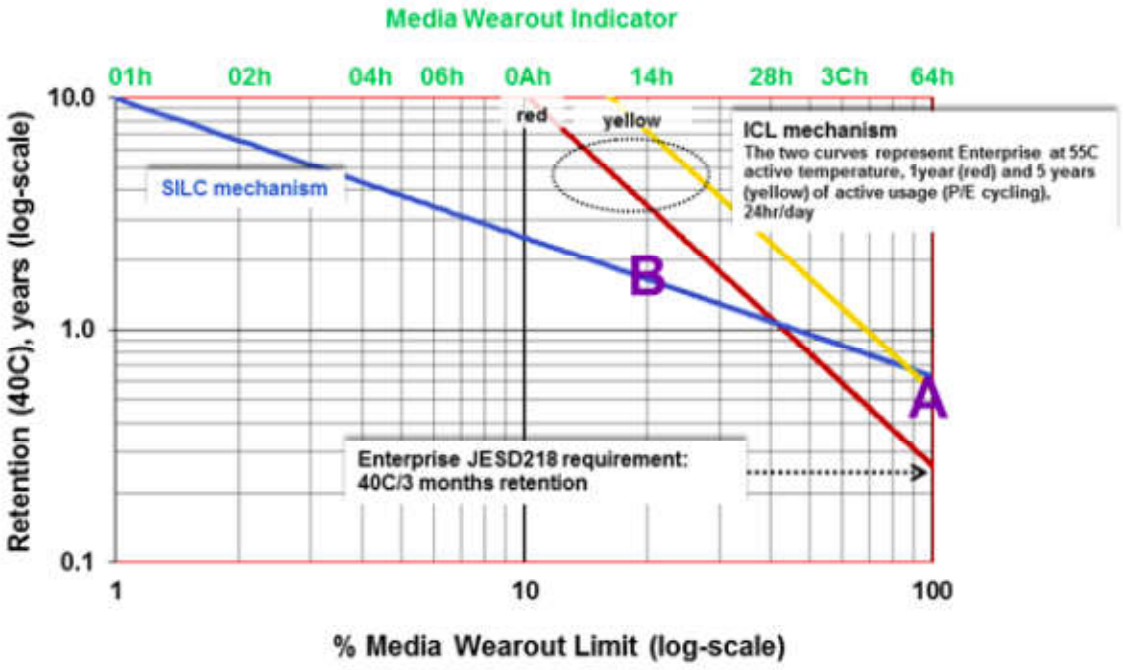
## 4.5 Data Retention – Intel® Solid-State Drive 910 Series

The data retention capability of the Intel SSD 910 Series is shown in Figure 5, which is similar to Figure 4 on page 16.

- The red line represents ICL for a P/E cycling time of 1 year at 55 ºC (JESD218A condition).
- The yellow represents ICL for a P/E cycling time of 5 years, thus it is shifted up from the red line due to the recovery effects mentioned earlier.
- The blue line represents SILC, which is independent of the P/E cycling time.
- The x-axis represents the number of P/E cycles seen by the NAND normalized to the Media Wearout Limit (which is closely aligned to the TBW rating in this case). The Media Wearout Indicator itself is also shown (in green) at the top of the plot.

Figure 5 shows that at 100% of the Media Wearout Limit, the 40 ºC retention times due to SILC and ICL are about 7 months and 3 months, respectively, and the overall retention capability is 3 months, limited by ICL.

**Figure 5. Data Retention – Intel SSD 910 Series**



In the case of the Intel SSD 910 Series, overall retention capability is limited by either ICL or SILC, depending on the usage conditions.

For example:

(A) The number of P/E cycles corresponding to the TBW of 14,000 TB specified in the *Intel® Solid-State Drive 910 Series Product Specification* for an 800 GB capacity SSD is close to 100% of the Media Wearout Limit. However, if TBW corresponds to host writes done over a period of 5 years, the ICL retention capability (yellow line) is about 6.5 months, denoted by the letter A in Figure 5. The retention due to SILC is greater, about 7 months, and the overall retention is limited by ICL in this case, about 6.5 months, which is much higher than the 3 months specified by JESD218A.

(B) Alternatively, considering the same 800 GB SSD but in the case where data is written to the SSD at the same rate but over a period of 1 year instead of 5 years, the number of P/E cycles would be at about 20% of the Media Wearout Limit. As denoted by letter B in Figure 5, the retention in this case would be about 1.6 years, and be limited by SILC.

In summary, the Intel SSD 910 Series meets the minimum enterprise JESD218 requirement of 3 months retention at 40 ºC, and is generally capable of better retention at more realistic usage conditions of longer than one year of active usage or smaller amount of TBW.



# 5.0 Summary

This application note provided a brief overview of a key reliability attribute for SSDs – data retention – and described key factors affecting underlying NAND data retention capability: the total amount of data written to the SSD (or P/E cycles on the NAND), the storage conditions, and the P/E cycling conditions.

SSDs are built with NAND flash memory, which has finite data retention capability. However the data retention capability of an Intel SSD is much better than what may be expected from basic NAND data retention capability. Data moves from internal SSD algorithms essentially refresh data often enough for data retention during active use to be a non-issue. Since these internal data moves are not possible when SSDs are powered off, data retention during non-use becomes the limiter for SSD retention capability, and thus was the focus of this application note.

Typically, there are two main mechanisms to consider with data retention: ICL (or detrapping) and SILC. One of the key points to remember when it comes to ICL is that it depends not only on the storage conditions, but also on the rate at which data is written to an SSD (or the P/E cycling time) due to recovery effects. Both the detrapping and recovery effects are strongly thermally activated mechanisms and thus make ICL highly dependent on storage *and* P/E cycling temperature. High temperature during storage makes ICL worse, while high temperature during P/E cycling improves it. The JEDEC standard JESD218A takes this fully into account while specifying the details of endurance and (high temperature) retention verification steps. The standard also defines and specifies methods for mechanisms such as SILC, which are not thermally activated and known to anneal out at very low temperatures, and thus cannot be accelerated using high temperature retention bakes.

Intel adheres to the JEDEC endurance and data retention stress methods and recommendations as described in the JESD218A standard to ensure its SSDs have sufficient retention capability. The retention capabilities of the client Intel SSD 320 Series and enterprise Intel SSD 710 Series presented in this application note are shown to not only meet but also exceed the stringent JEDEC standard at their maximum endurance ratings specified in their product specifications. Additionally, data will be retained effectively indefinitely during active use because of the special internal drive algorithms used to maximize the performance, quality, and reliability of Intel SSDs.

# 6.0 Reference Documents

Table 2 lists the standards and specifications referenced in this application note.

## Table 2. Standards References

| Document | Document No./Location |
|---|---|
| 1. Solid State Drive (SSD) Requirements and Endurance Test Method (JESD218) | http://www.jedec.org |
| 2. Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test (JESD22-A117) | http://www.jedec.org |
| 3. Failure Mechanisms and Models for Semiconductor Devices (JEP122) | http://www.jedec.org |
| 4. Solid State Drive (SSD) Endurance Workloads (JESD219) | http://www.jedec.org |

Table 3 lists the documents referenced in this application note.

## Table 3. Reference Papers

| Document | Location |
|---|---|
| 1. Mielke, N.; Belgal, H.P.; Fazio, A.; Meng, Q.; Righos, N.; , "Recovery Effects in the Distributed Cycling of Flash Memories," *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International* , vol., no., pp.29-35, 26-30 March 2006 | http://ieeexplore.ieee.org |
| 2. Mielke, N.; Belgal, H.; Kalastirsky, I.; Kalavade, P.; Kurtz, A.; Qingru Meng; Righos, N.; Jie Wu; , "Flash EEPROM threshold instabilities due to charge trapping during program/erase cycling," *Device and Materials Reliability, IEEE Transactions on* , vol.4, no.3, pp. 335- 344, Sept. 2004 | http://ieeexplore.ieee.org |
| 3. Belgal, H.P.; Righos, N.; Kalastirsky, I.; Peterson, J.J.; Shiner, R.; Mielke, N.; , "A new reliability model for post-cycling charge retention of flash memories," *Reliability Physics Symposium Proceedings, 2002. 40th Annual* , vol., no., pp. 7- 20, 2002 | http://ieeexplore.ieee.org |

# 7.0 Additional Information

Table 4 lists additional documentation available for Intel SSDs.

## Table 4. Related Documentation

| Document | Document No./Location |
|---|---|
| Intel® Solid-State Drive 320 Series Product Specification | 325152 |
| Intel® Solid-State Drive 710 Series Product Specification | 325633 |



# 8.0 Revision History

| Date | Revision | Description |
|---|---|---|
| December 2011 | 001 | Initial release |
| June 2012 | 002 | Added Intel® SSD 910 Series Data Retention (section 4.5) |